Amendments to the Figures

Figures 1-2 have been amended by adding the label "(BACKGROUND)" below each Figure, as required by the Examiner. Replacement Sheets (as required by 37 C.F.R. 1.121(d)) are attached to this Amendment.

Remarks

Claims 1, 4, 6, 7 and 9 have been amended. The amendments to claim 4 include changes to provide antecedent basis for one or more terms in claim 8 and to remedy a grammatical error. Claim 6 has been amended to delete "the supporting structures being inserted into the positioning holes," thereby rectifying the dependent form of claim 9. Claim 7 has been amended to maintain consistency with the specification and to remedy a grammatical error. Claim 9 has been amended to remedy a typographical error.

The Rejections of the Claims under 35 U.S.C. § 103

The rejection of Claims 1-4 and 7 under 35 U.S.C. § 103(a) as being unpatentable over Hara taken with Hong, and the rejection of Claims 5, 6, 8, and 9 under 35 U.S.C 103(a) as being unpatentable over Hara taken with Hong, further in view of Lee, are respectfully traversed.

The invention recited in claim 1 is structurally different from Hara. The presently claimed invention concerns a semiconductor chip (e.g., see 130 in FIGS. 3B and 5B) electrically connected to lead frames (e.g., 134 in FIGS. 3B and 5B) and outer leads (e.g., 120 in FIGS. 3A-3B and 4A) connected to metal lines (e.g., 140 in FIGS. 3B and 5B), the metal lines being connected to the lead frames. That is, the semiconductor chip is electrically connected to outer leads. In contrast, Hara does not appear to disclose that leads (51) connected to an external structure (54) are connected to an internal semiconductor chip through metal lines.

Secondly, the metal lines of the presently claimed invention are functionally different from those of Hong. As the Examiner pointed out, Hara does not appear to disclose metal lines. Furthermore, the metal lines (27) disclosed by Hong function to make a relatively simple connection between a semiconductor chip (10) and outer leads (52). By contrast, the metal lines of the present claims have a much different function from those of Hong:

1. The metal lines of the present claims connect a semiconductor chip, its own outer leads and outer leads of another package. As shown, for example, in Fig. 3B, the metal lines (e.g., 140) are connected to outer leads (e.g., 120) through via holes

(e.g., 142) formed at a bottom surface of the package. Further, the metal lines are connected to outer leads of another package through grooves (e.g., 110) formed at a top surface of the package. So, the metal lines make it possible for a semiconductor chip (e.g., 130) to communicate with another packaged IC without any need for further substrates for connecting semiconductor chips.

2. The metal lines of the present claims make it easy to change a width between two rows of outer leads (e.g., 120 shown in Fig. 3A). In the case of Hong, in order to change the width, it is necessary to redesign leads (52) and a substrate (20). Since the leads (52) are attached to a recess portion (26) of the substrate (20), if the width needs to be smaller, a size of the recess portion (26) has to be bigger, and vice versa. According to the present invention, on the other hand, merely changing the positions of via holes enables changing the widths between leads. The structure of a package body (e.g., 100) does not need to be redesigned.

Thirdly, the present invention enables stacking without limitation of package size. Figs. 4 and 8 of Hara are cross-sectional views showing the processes of resin encapsulation of the semiconductor device in accordance with the first and the second embodiments. According to those processes, outer leads (33, 55) are formed at sides of the package. In this case, an upper package (53) should be smaller than a lower one (49) because outer leads (55) of the upper package (53) apparently have to be inserted into a linking hole (50) formed at an upper surface of a lower package body (49). This is apparent from Fig. 5. On the other hand, in the presently claimed invention, via holes (e.g., 142) through which outer leads (e.g., 120) are formed and grooves (e.g., 110) through which outer leads of another package are connected are formed at top and bottom surfaces, respectively. Therefore, even though an upper package may be bigger than or same as a lower package, as long as the width and pitch of the outer leads are same, they can be easily connected to each other using the present invention.

For essentially the same reasons, the invention of claim 4 (which recites technical features similar to those of claim 1) is patentable over Hara in view of Hong. Therefore, it is

respectfully submitted that independent claims 1 and 4 define a patentable invention over Hara taken with Hong and are, therefore, believed to be allowable.

It is also believed that claims 2 and 3 (which depend on claim 1) and claims 5 to 9 (which depend directly or indirectly on claim 4) are allowable for the same reasons indicated with respect to amended claims 1 and 4, respectively. Furthermore, because of the additional features recited therein which, when taken alone and/or in combination with the features recited in amended claims 1 and/or 4, the invention defined in claims 2-3 and 5-9 is further removed from the disclosures of the cited references.

Consequently, this basis for rejection is believed to be unsustainable, and should be withdrawn.

The rejection of Claims 5, 6, 8, and 9 under 35 U.S.C 103(a) as being unpatentable over Hara taken with Hong, further in view of Lee, is respectfully traversed.

Lee discloses a stacked semiconductor package including a plurality of semiconductor devices stacked over one another and having outer leads, which are extended from sides of the devices and bent downwardly. A plurality of supports are vertically interposed between the outer leads. The supports electrically connect the outer leads in vertical direction only (Abstract).

Lee, like Hara and Hong, is silent with regard to outer leads connected to metal lines through via holes (Claim 1), or outer wires connected to the semiconductor chip through via holes, metal lines and lead frames (Claim 4), where the metal lines are connected to the lead frames (Claims 1 and 4). Thus, Lee does not appear to cure the deficiencies of Hara and Hong with regard to the present Claims 1 and 4.

Therefore, claims 5, 6, 8, and 9 (which include all of the limitations of independent claims 1 and 4) are patentable over Hara taken with Hong and are, therefore, believed to be allowable. Furthermore, because of the additional features recited therein which, when taken alone and/or in combination with the features recited in amended claims 1 and/or 4, claims 5, 6, 8, and 9 are further removed from the disclosures of the cited references.

Consequently, this ground of rejection is believed to be unsustainable, and should be withdrawn.

The Rejection of Claim 8 under 35 U.S.C. § 112, Second Paragraph

The rejection of Claim 8 under 35 U.S.C. § 112, second paragraph has been obviated by appropriate amendment.

The Objections to the Drawings and to Claim 9

The objections to the drawings and to Claim 9 have been overcome by appropriate amendment.

Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are believed to be overcome, and the application is believed to be in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,

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